REMARKS

Applicant appreciates the thorough examination of the present application that is reflected in the Official Action of March 2, 2004. Applicant also appreciates the Examiner's indication that Claim 6 would be allowable if rewritten in independent form. Rather than rewriting Claim 6 in independent form, independent Claim 1 has been amended to clearly recite that the plug and the conformal monocrystalline silicon layer comprise two different materials. Accordingly, Claim 1 and the dependent claims that depend therefrom are patentable for the reasons that now will be described.

In particular, Claim 1 recites:

> 1. A vertical field effect transistor comprising:
> a microelectronic substrate including a trench, the trench defining a sidewall;
> a conformal monocrystalline silicon layer on the sidewall of the trench, the conformal monocrystalline silicon layer on the sidewall of the trench including a drain region adjacent the substrate, a source region remote from the substrate and a channel region between the source and drain regions;
> a plug comprising insulating material in the trench that includes the conformal monocrystalline silicon layer on the sidewall thereof;
> a gate insulating layer adjacent the channel; and
> a gate electrode on the gate insulating layer opposite the channel. (Emphasis added.)

As clearly shown by the underlined language of Claim 1, two different structures are provided in the trench: a conformal monocrystalline silicon layer on the sidewall of the trench, and a plug comprising insulating material in the trench. In order to highlight the fact that the plug is different from the conformal monocrystalline silicon layer, Claim 1 has been amended to recite "a plug comprising insulating material". Support for this amendment may be found, for example, at Page 11, line 31-Page 12, line 15 of the present application, and more specifically at Page 12, lines 13-15.

In sharp contrast, in Hergenrother et al. U.S. Patent 6,027,975, a single silicon plug is provided in the trench. See, for example, Hergenrother et al., Column 9, line 53-Column 10, line 3:

> Referring to FIG. 3E, the window **225** is then filled with a crystalline semiconductor material (e.g. silicon) **230**. Techniques for forming single crystalline silicon in windows are well known to one skilled in the art. In one embodiment, epitaxial silicon is deposited selectively in the window **225**. In another embodiment, amorphous silicon is deposited over the entire substrate surface and all but the silicon **230** deposited in the window **225**, and a small portion **231** at the top of the window, is removed. The amorphous semiconductor material is then recrystallized by annealing the substrate.

> The crystalline semiconductor plug **230** formed in the window **225** becomes the channel of the device (**260** in FIG. 3P). Therefore, the crystalline semiconductor plug **230** is doped. It is advantageous if the dopant for channel region **260** is introduced in situ as the plug **230** is being formed. However, implantation of the dopant is also contemplated as suitable. (Emphasis added.)

Accordingly, a crystalline semiconductor plug **230** is formed in the trench. Region **260** of FIG. 3P denotes the channel region within the crystalline semiconductor plug **230**. However, the channel region **260** is a portion of the crystalline silicon plug **230**, and not a separate plug comprising insulating material.

In view of the above, Hergenrother et al. does not anticipate Claim 1, and it would not be obvious to modify Hergenrother et al. to provide a separate plug comprising insulating material in the trench that includes the conformal monocrystalline silicon layer on the sidewall thereof, as recited in Claim 1. Claim 1 is thereby patentable. Claims 2-7 are patentable at least as depending from Claim 1. Moreover, as already noted by the Official Action, Claim 6 is independently patentable. Claim 6 has also been amended to provide proper antecedent basis for "insulating material" and to eliminate the typographical error in "transistors", to thereby overcome the claim objection. Finally, a new Abstract is being supplied that is less than 150 words long.

Applicant is also filing concurrently herewith a "Second Request for Corrected Filing Receipt". As shown therein, Applicant respectfully requests the Filing Receipt to be corrected to reflect that the parent application claims the benefit of Provisional Application Serial No. 60/252,306, filed 11/22/2000.

Accordingly, Applicant respectfully requests allowance of the present application and passing the application to issue.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 15, 2004.

Susan E. Freedman
Date of Signature: April 15, 2004

VERTICAL FIELD EFFECT TRANSISTORS INCLUDING CONFORMAL MONOCRYSTALLINE SILICON LAYER ON TRENCH SIDEWALL

Abstract

A vertical field effect transistor includes a microelectronic substrate having a trench, the trench defining a sidewall. A conformal monocrystalline silicon layer is provided on the sidewall, including a drain region adjacent the substrate, a source region remote from the substrate, and a channel region between the source and drain regions. A plug is provided in the trench. A gate insulating layer is provided adjacent the channel and a gate electrode is provided on the gate insulating layer.